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(54) Stage Lighting Control System

(57) A stage lighting control system has a main processor unit and a portable desk controller with a local microprocessor (21) which scans the dimmer control contacts in the desk and transmits changed state control data to the main processor as an asynchronous serially coded signal on a low capacity link. This enables the controller to be conveniently located remote from the rack. Changed display data is developed by a V.D.U. interface in the main processor for transmission on the link as standard composite video to a V.D.U. (51). Output to the dimmers circuitry is through channel processors controlling groups of dimmers for data formatting. Lighting level information is recorded using a channel code. Patching means enable differing arrangements of dimmers circuitry to be controlled in accordance with the original record.

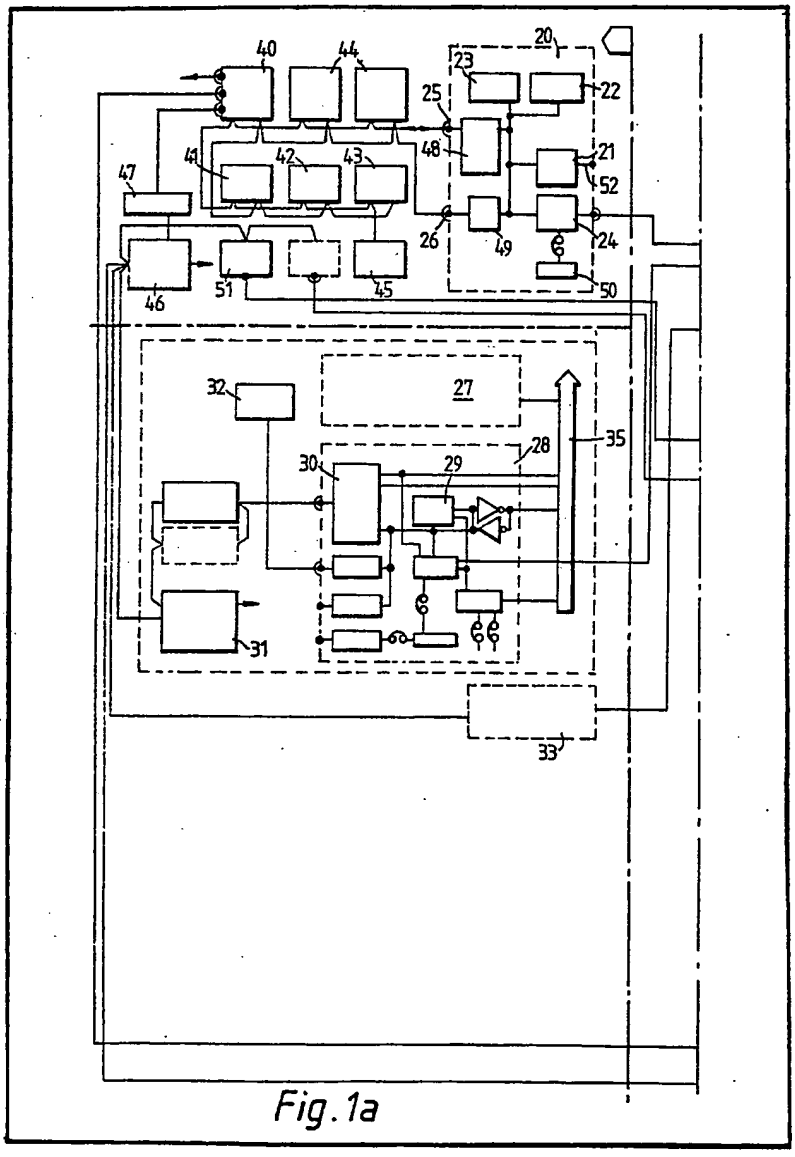

Fig. 1a

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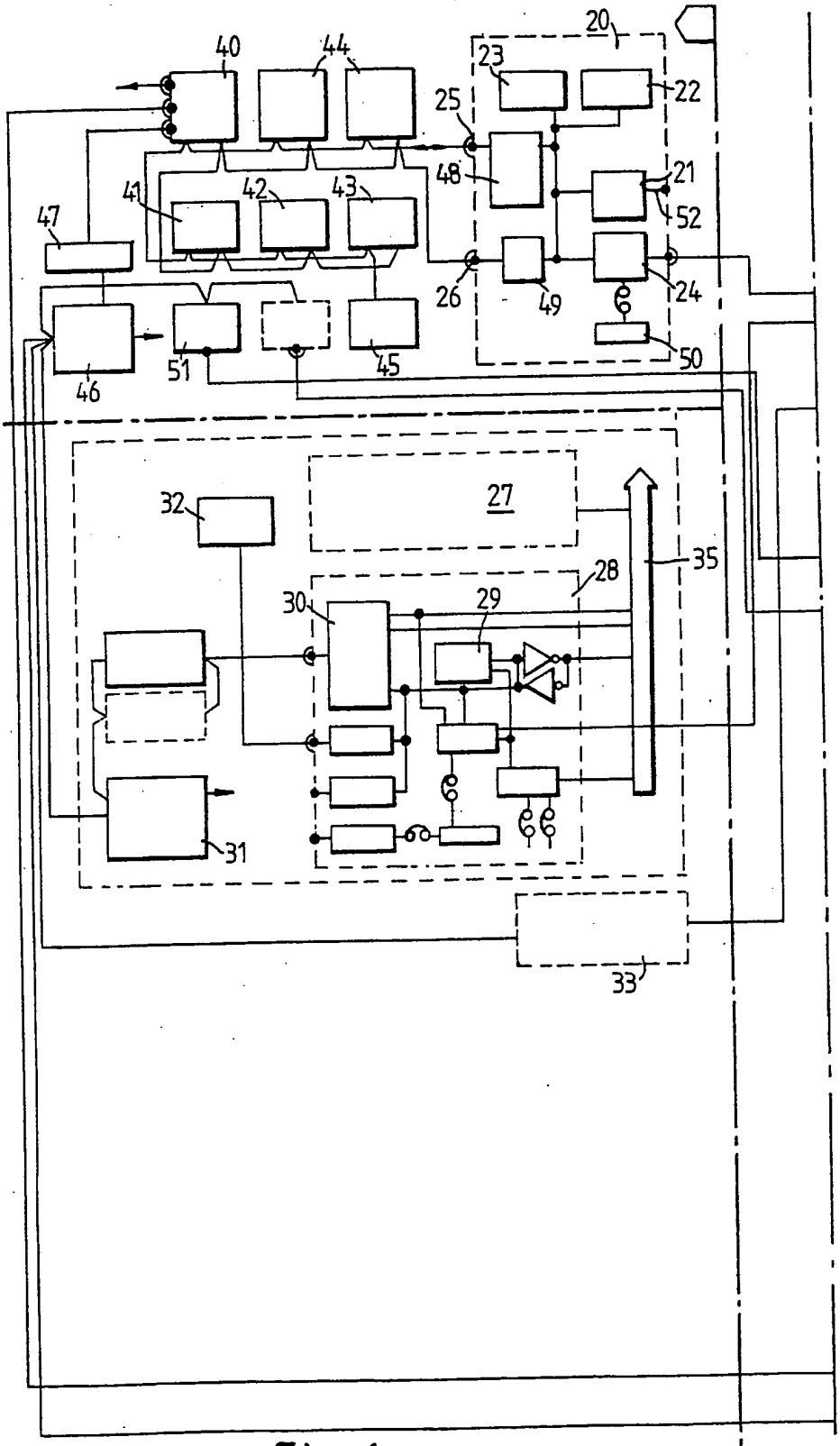
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Fig. 1a

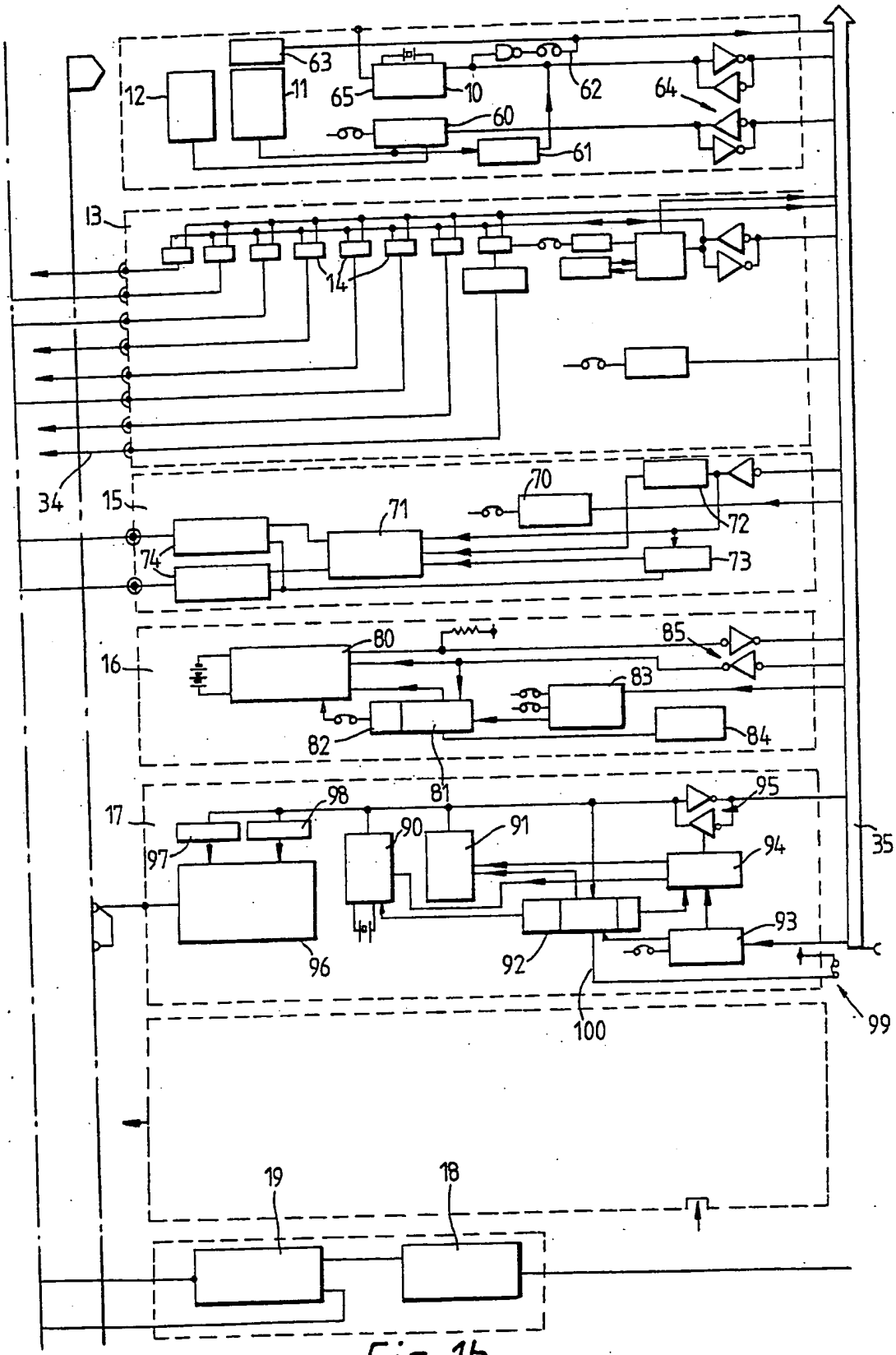
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Fig. 1b

SPECIFICATION

Stage Lighting Control System

This invention relates to a stage lighting control system.

In the field of stage lighting, it is known to provide a memory facility into which can be stored information relating to the dimmer levels necessary to produce various lighting effects. This information is pre-stored, for example during a rehearsal, in a main processor herein referred to as the rack, and can be recalled (played back) during a performance by operating (cueing) various controls such as faders on a control console. It is preferably possible for the control console to be separable from the rack in order to permit its location at a chosen site from which the stage is visible. By means of such a memory control system complex lighting effects can be achieved, involving the simultaneous adjustment of the levels of many individual dimmers by the use of linked controls referred to as masters, which effects would otherwise be virtually impossible to synthesize at the time owing to the large number of simultaneous controlled adjustments which would be necessary.

It is an object of the present invention to provide an improved memory lighting control system, in particular enabling limited capacity microprocessors to be employed to achieve at least the same operational and computational capacity as mini-computers which have hitherto been employed.

According to one aspect of the present invention, there is provided a stage lighting control system comprising a main processor unit including a memory for storing information relating to the dimmer levels necessary to produce various lighting effects; a portable controller having read/write selection means and a range of dimmer level control elements, said portable controller also incorporating a local processor unit adapted to scan the range of control elements to detect changes of state therein, an address memory for storing address data relating to the memory in the main processor unit, and a multiplexer for producing a coded signal containing selected address data and changed state data; and a low capacity cable link connecting the main processor unit with the portable controller.

Thus, in systems used hitherto, it has been the practice for the main processor in the rack to include, as part of its operating program, a facility for scanning the controls at the control console. It was therefore necessary to provide a high capacity data link (at least 300 k bytes per second) between the rack and the control console in order to avoid slow response within the main processor. The large connecting cable containing parallel address and data wires was thus very large and cumbersome, and severely limited the portability of the control console.

However, in accordance with the invention, in which only the changed state data is transmitted, the information speed required is only about 2 k bytes per second for combined address and control element data, and for this speed of transmission the data can readily be time multiplexed into a standard asynchronous serial code for transmission to the rack on a two wire circuit. The rack processor is freed of the part of its program originally required for scanning, assisting its processing efficiency.

The transmission of changed display data from the rack to a display unit forming part of the control console can be effected in similar manner. Thus, the control console can be connected to the rack by a link circuit consisting of only four wires, which can easily be extended to a considerable length (such as 500 to 1000 m), enabling the control console readily to be sited at any preferred location within the theatre.

In a preferred embodiment of the invention, the main processor unit has a large plurality of coded output channels for providing level control signals to a corresponding plurality of dimmers and a portion of the memory stores under coded addresses information relating to the dimmer levels necessary to produce various lighting effects; and the signals read from said memory portion are fed to the dimmer output channels through a patching means which can be patched to alter the dimmer channel which is controlled when a level control signal for a particular coded address in said memory portion is addressed.

In a conventional memory lighting control system, it has been usual to number the dimmers contiguously from 1 to a maximum, and to store lighting levels for each respective dimmer against its allotted number. This is satisfactory when the memory is specifically tailored to one particular theatre and is intended for use solely in that theatre. However, if the memory is required for use in a number of theatres, for example when a production is on tour, it is a disadvantage that in different theatres the same numbered dimmer may cause different lighting effects.

In addition, wiring errors can occur whereby a dimmer having a particular number does not produce the effect that it should.

In the present invention, lighting levels are memorised in association with channel codes, i.e. channels coded by number or by alpha-numeric identity for example. Thus, when the memory is used in a different theatre, or when wiring errors must be dealt with, the patching means can be used to ensure that the original channel code (address in the memory) controls a different dimmer (numbered or otherwise coded output channel) to achieve the original lighting effect. This has the advantages that operators' notes and lighting designs can be kept unchanged with different arrangements of the dimmer's wiring.

More especially, this aspect of the invention is important in connection with the provision of a portable memory such as a floppy disc peripheral to the main control system but which can be interfaced with the rack. In this case, there will be provided means on the controller for initiating

transfer of information between the memory in said main processor unit and said portable memory, optionally including patching information, and second means on the controller enabling the portable memory to control the dimmers through the patching means.

According to still another aspect of the present invention, there is provided a stage lighting control system comprising a main processor unit which comprises a memory having a current store and at least one preset store for containing information relating to the dimmer levels necessary to produce various lighting effects, an executive microprocessor for exchanging information with a controller having read/write selection means and a range of dimmer level control elements, a plurality of groups of output channels for providing level control signals to a plurality of dimmers, and a plurality of slave microprocessors, one for each group of output channels, each for performing hierarchical calculations on information data fed from the current and preset store or stores in accordance with instructions contained in an associated random access memory updated from the executive microprocessor.

Preferably, the hierarchical calculations are performed cyclically and are output from the slave microprocessor of each group through analogue sample and hold circuits, one such circuit for each dimmer channel. In addition, each group of output channels preferably has a channel register serving to index an address store in a memory for the slave microprocessor, each channel register being duplicated with a positional offset so that the respective channel processors respond to different coded address sections in the dimmer level memory.

Thus, in one arrangement of the lighting control system in accordance with the invention, each dimer is controllable by a "move fade" in the stage (current) output store and/or a highest-take precedence output from a plurality of, for example ten, preset stores, each individually mastered. A move fade may also occur in any one preset store. The dimmers level is calculated on a repetitive cycle of approximately 30 to 50 ms (sufficiently short to avoid visible stepping on the lights as the fade progresses), and the output to the dimmers is fed through the analogue sample and hold circuits.

The move fade is calculated for each channel as follows:

Mn=movement of master since preceding calculation (ε Mn=256)

Sn=preceding stage store level

Sn+1=stage store level after new calculation

I=fade increment for particular dimmer (value=start value less destination value) whence

$$Sn+1=Sn+\frac{M\times I}{256}$$

This is combined on a highest-takes-precedence basis (Λ) with the mastered preset stores as follows:—

MPx=Preset store master x(0→256)

Px=Preset store x(0→255)

giving a dimmer output expression of:

$$Output=Sn+1\,\Lambda MP_1 . P_1 \Lambda MP_2 . P_2 \cdots\cdots \Lambda MP_{10} . P_{10}$$

Additionally, an identical calculation takes place on one preset store.

This calculation on a fast 8-bit microprocessor takes just under 1 mS. Conveniently, therefore, each output channel group may consist of 48 output channels, for which the dimmers outputs are calculated by the slave microprocessor for the group, a RAM memory array containing the operating program and the associated stores. The executive microprocessor performs the main system logic operations and updates the RAM memory arrays.

Such a system has the advantage that it can be expanded as necessary by the addition of output channel groups. Assuming a large system of say 16 output channel groups, the apparent address size is reduced by the provision of the channel registers which index the RAM memory array. With the associated positional offset, the full range of 768 outputs RAM (16x48) can be accessed by only 64 addressed bytes and the register.

A practical arrangement of memory lighting control system in accordance with the invention is illustrated in the accompanying drawing.

In this drawing, the control console labelled "desk" is at the upper left hand corner. The main processor labelled "rack" is on the right, and is connected to the control console through a low data capacity 4 wire link which may readily be extended up to 1000 m. The bottom left hand side of the drawing illustrates a portable memory labelled "floppy disc" which is peripheral to the main system but can be interfaced with the rack to provide a back-up memory.

The rack essentially consists of a basic processor crate containing a host or executive microprocessor 10 incorporating PROM 11 and RAM 12, a serial interface board 13 containing asynchronous communications interface adaptors 14, a dual visual display unit interface board 15, a CMOS RAM lighting level memory board 16, and a plurality of channel processor boards 17 (of which only one is shown) each having 48 output channels. An optional interface permits the CMOS memory to be replaced with a ferrite core memory. The crate also contains a power supply unit 18 and a system power control 19.

In the remote desk, an interface board 20 contains a local microprocessor 21 with associated PROM 22 and RAM 23, outputting through an asynchronous serial link 24 to the rack. Two ports 25, 26 connect to the control panel motherboards to scan the contacts of the various dimmers level controls and the drive mimics.

In the floppy disc drive, an identical microprocessor 27 to that in the rack controls an

interface board 28 containing supplementary RAM 29 and a drive controller 30 providing up to two drives. A power supply unit 31 is incorporated, together with a panel 32 presenting status and allowing initialization of diskettes.

In addition, the drawing shows a printer 33 interfaced with the rack and riggers connections 34 interfaced with the rack in accordance with required standards. In all instances, the interfaces incorporate the current loop asynchronous serial links ensuring the necessary signals isolation at the processor bus 35.

In more detail, the desk has a sub-panel 40 of memory number selection switches for selecting by memory number, as distinct from dimmer number, the memory channel into and from which information is to be written and read. A channel controller 41 enables one or more selected channels to be controlled, in association with a master wheel fader and a plurality of group masters designated 42. Generally similar fade controls are available at a preset store controller 43. Two automatic playbacks are provided, as indicated at 44. At least one visual display unit 51 is operative to indicate active channels, with the option to display channel levels. An alpha keyboard 45 enables supplementary matter to be displayed. A desk power supply unit 46 is connected to the motherboards through a lamp regulator 47.

Controls of the above-described form are generally conventional, and need not be described in detail. The essential feature of the desk, as far as the present invention is concerned, lies in the interface board 20.

Here, the local memory 22, 23 is programmed such that the local microprocessor 21 cyclically scans the contacts of the various controls at the desk to produce a signal for transmission to the rack. The only data transmitted is that representing a change of state at the control contacts. The changed state data is then transmitted in an asynchronous serial code comprising pairs of 8 bit bytes, the first indicating the address of the data, the second the actual data. Changed state data is transmitted immediately, together with a mimic update transmission of all bytes, if requested by the rack to correct any errors. Once each cycle a sync. response byte is transmitted to the rack responsive to receipt of a sync. byte from the rack.

The above described desk to rack asynchronous serial code transmission is effected on a simple two wire link at a rate of about 2k bytes per second, fully sufficient to the processing speed required for proper lighting control.

The drawing also shows the buffers and decoders unit 48 provided in the interface board 20 at the digital port 25 connecting to the motherboards, the A/D and D/A converter unit 49 at the analogue port 26 connecting to the motherboards, the timer 50 providing serial data timing of 300—19,200 band, the asynchronous serial output adaptor 24 providing opto-isolation, and the processor test port 52.

The executive microprocessor 10 in the rack is programmed to process the changed state data received from the remote desk and to provide appropriate signals to the CMOS memory 16 and channel processor 17. However, this microp ocessor m0 does not perform all the nece sary login operations necessary to derive the dimmr control ignals. The signals fed to the channel processor 17 are intermediate signals which enable further logic operations to be performed to produce such dimmer control signals. The drawing also shows the address decoder 60 for executive microprocessor 10, the PROM delay circuit 61, the sync. and reset circuit 62 with its associated logic circuit 63, the tri-state drive and low power receive circuits 64, and the processor test port 65.

The next unit shown in the rack is the serial interface board 13. This unit is not of primary importance in relation to the present invention and will not be described in detail. Essentially it provides the optional input and output connections to the rack from peripheral equipment. One such connection will be mentioned specifically, and this is the connection to the floppy disc.

The rack also contains the dual visual display unit (V.D.U.) interface 15, which includes patchable address decoder 70, write only RAM 71 containing character codes and attributes and addressed by attribute register 72, V.D.U. timer 73 timing the production of the dot character array, and dual V.D.U. character generators 74. This write only unit generates the display information in accordance with display signals received from the channel processors 17 and transmits the generated character signals back to the V.D.U.s 51 in the control desk. The display signals form a composite video signal, compatible with standard video monitors and display the channels in use and their levels on the V.D.U.s. A separate link transmits changed display data from the rack to the desk, this data being time multiplexed into a serial code transmitted at the rate of 2k bytes per second.

The CMOS RAM lighting level memory board 16 stores the dimmer levels to be recalled under the control of the desk to fade the dimmers through the intermediary of the channel processors 17. This CMOS memory 80 can optionally be replaced by a ferrite core memory. The memory 80 is accessed by a page register 81 having a memory lock 82 and served by a patchable address decoder 83 and a page switch 84. Input/output is via tri-state drive-low power receive circuits 85. The CMOS memory 80, preferably battery maintained, is divided into 16 overlapping areas providing an economy of executive address utilisation, together with an address area for channel identification.

The final unit to be discussed in the rack is the channel processor 17. This comprises a slave microprocessor 90 associated with a RAM direct access memory 91, a resettable channel register 92 addressed through a decoder 93, an

arbitration logic circuit 94, input/output connections 96 to the procesor bus, an output to the dimmers circuitry through analogue sample and hold circuits 96 preceded by channel number and channel level regulators 97 and 98. Associated with the channel register 92 is a position offset patch 99.

Each channel register 92 handles two adjacent bytes respectively defining the channel group (up to 16) and the channel number (1 to 48) within the group, while the RAM 91 address area is divided into four groups of 16 stores for each of the 48 address channels. Thus by duplicating each channel register with a position offset 100, the full range of RAM locations (16x4x16x48) can be accessed by only 64 addressed bytes and a register. It is to be noted that the register 92 is addressed separately to the RAM 91 and is not accessible to the slave processor 90. The RAM 91 also contains operational instructions for the logical hierarchy operations to be carried out by the processor 90. The highest-takes-precedence processing which is effected has been previously described. In addition, the RAM 91 contains a copy of the two output registers which define the sample and hold channel number and level data utilised in the regulators 97, 98 feeding the sample and hold output circuits 96. These bytes written into these two output regulators may be recalled either by the executive microprocessor or the slave microprocessor.

The above-described arrangement also provides a patch facility whereby it is possible to redirect levels read from the CMOS memory (or floppy disc), for identified channels, to alternative channels, before action by the channel processors. This enables, for example, similar lighting effects to be achieved with differing arrangements of the dimmers circuitry.

A separate patch facility, controlled by an emergency switch at the remote control desk, effects a change in the source of memory data, substituting the floppy disc for the CMOS or ferrite memory. This switch can thus be used as a back up in the event of main memory failure.

Claims

1. A stage lighting control system comprising a main processor unit including a memory for storing information relating to the dimmer levels necessary to produce various lighting effects; a portable controller having read/write selection means and a range of dimmer level control elements, said portable controller also incorporating a local processor unit adapted to scan the range of control elements to detect changes of state therein, an address memory for storing address data relating to the memory in the main processor unit, and a multiplexer for producing a coded signal containing selected address data and changed state data; and a low capacity cable link connecting the main processor unit with the portable controller.

2. A system according to claim 1, wherein the selected address and changed state data is time multiplexed into an asynchronous serially coded signal and transmitted to the main processor unit on a two wire link.

3. A system according to claim 2, including a display unit at the portable controller, wherein display data produced in the main processor unit is incorporated into a composite video signal for transmission to the display unit, and changed display data is transmitted from the main processor unit to the portable controller as a serially coded signal on a separate two wire link.

4. A system according to claim 1 or claim 2 or claim 3, wherein the main processor unit has a large plurality of coded output channels for providing level control signals to a corresponding plurality of dimmers and a portion of the memory stores under coded addresses information relating to the dimmer levels necessary to produce various lighting effects; and the signals read from said memory portion are fed to the dimmer output channels through a patching means which can be patched to alter the dimmer channel which is controlled when a level control signal for a particular coded address in said memory portion is addressed.

5. A system according to claim 4, including a portable memory which can be interfaced with the main processor unit, and means on the portable controller for initiating transfer of information between the memory in said main processor unit and said portable memory, optionally including patching information, and second means on the controller enabling the portable memory to be used to directly control the dimmers.

6. A stage lighting control system comprising a main processor unit which comprises a memory having a current store and at least one preset store for containing information relating to the dimmer levels necessary to produce various lighting effects; an executive microprocessor for exchanging changed state information with a portable controller having a local processor, read/write selection means and a range of dimmer level control elements; a plurality of groups of output channels for providing level control signals to a plurality of dimmers; and a plurality of slave microprocessors, one for each group of output channels, each for performing hierarchical calculations on information data fed from the current and preset store or stores in accordance with instructions contained in an associated random access memory updated from the executive microprocessor.

7. A system according to claim 6, wherein the hierarchical calculations are performed cyclically and are output from the slave microprocessor of each group through analogue sample and hold circuits, one such circuit for each dimmer channel.

8. A system according to claim 6 or claim 7, wherein each group of output channels has a channel register serving to index an address store in a memory for the slave microprocessor, each channel register being duplicated with a positional offset so that the respective channel

processors respond to different coded address sections in the dimmer level memory.

9. A stage lighting control system substantially as hereinbefore described with reference to the accompanying drawing.

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